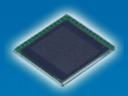
PIXELPLUS

PX6130KA 1.3MP Product Brief



The PX6130KA is single chip of CIS and ISP. It has excellent noise performance for low light condition and high dynamic range supported by 2-exp line based HDR mode up to 120dB. It has an advanced safety mechanisms of ASIL-B grade for Automotive.

The PX6130KA is single chip of 1.3MP image sensor and ISP for automotive viewing applications. The image sensor delivers high dynamic range up to 120 dB by using dual conversion gain (DCG) method and the ISP enables high quality HDR imaging with advanced image technology. The PX6130KA supports sufficient safety mechanisms of ASIL-B grade.

The HDR image shows no saturation or loss of shadow detail in situations of dramatic contrast such as when entering or exiting tunnels.
The low noise performance enables surround-view and rear view camera, E-mirror applications with excellent image quality.

Applications

- 360° Surround View Monitoring System (SVM)
- Rear View Camera
- E-Mirror

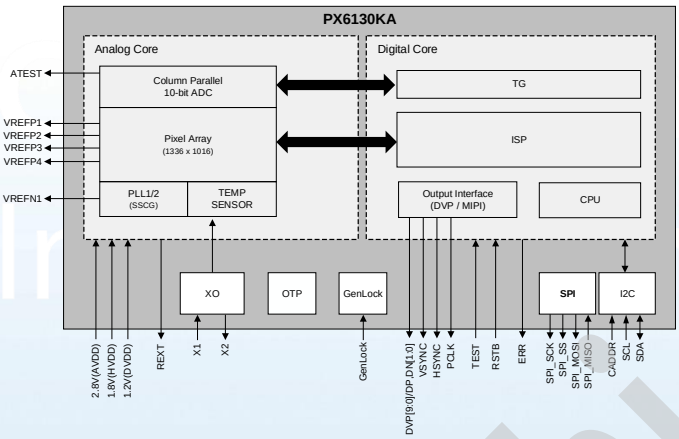
Product Features

- ASIL-B safety feature / AEC-Q100
- 120dB HDR with 2-Lane MIPI / DVP Combo output
- YUV / RAW output format
- Low fixed pattern noise of 3.0um BSI Pixel
- Low readout noise
- Programmable frame size, window size, and exposure
- External synchronization support (Genlock)
- One-time programmable memory (OTP)
- AR coating Glass
- Active Dummy Array for offset correction
- Spread Spectrum Clock Generation (SSCG)
- Dead Pixel Correction (DPC)
- Lens Shading Correction (LSC)
- Combine
- Tone Map
- Color Interpolation and Correction
- Denoise
- Dehaze
- Gamma Correction
- Edge Enhancement
- AE/AWB

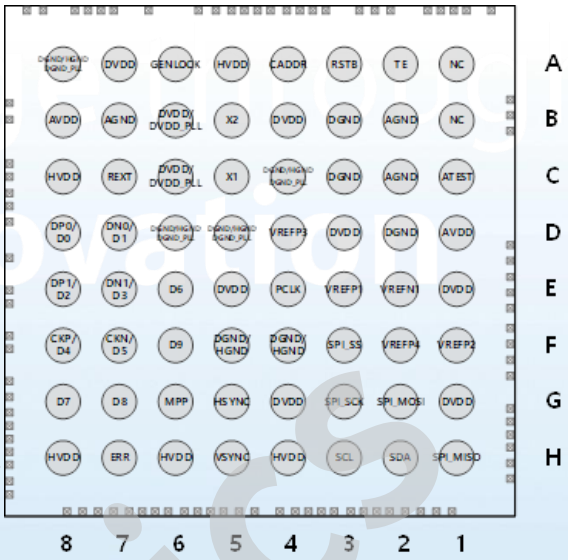
Technical Specifications

Parameter	Typical value
Pixel size	3.0 um x 3.0 um
Effective pixel array	1336(H) x 1016(V)
Effective image area	4.008 mm x 3.048 mm
Optical format	1/3.75 inch
CRA	23.7 °
AR coating glass	O (option)
Input clock frequency	27 MHz
Output interface	2-Lane MIPI / DVP Combo with RAW / YUV data
Max. frame rate	HDR 30 fps
Dark signal	TBD e/sec
Sensitivity	TBD V/Lux·s
Power supply	HVDD(DVP) : 1.7 ~ 1.9V HVDD(MIPI) : 1.7 ~ 1.9V
	AVDD : 3.0 V
	DVDD : 1.2 V
Power consumption	TBD
Operating temp.	-40 ~ 105 °C (Ambient)
Max. dynamic range	120 dB
SNR	TBD dB
Package type	A-CSP
Package size	5.950mm x 5.950mm x 0.870mm

Functional Block Diagram



A-CSP Ball Map



- Chip size : 5950 um x 5950 um, 64 ball

A-CSP Ball Description

Ball	Ball Name	IO	Pull up/ Pull down	Ball Description
A1	NC	-	-	-
A2	TE	I	-	Chip test enable
A3	RSTB	I	-	System reset must remain low for at least 8 master clocks after power is stabilized. When the chip is reset, all registers are set to their default values.
A4	CADDR	I	-	I2C slave device address selection pin. Multi-purpose pin function is supported. When Multi-purpose pin function mode is enabled, I2C slave device address selection pin is tied to GND internally. (ERR (Alarm)/UART Rx/PWM3/GPIO[9])
A5	HVDD	P	-	IO VDD 1.8V DC (MIPI), 1.8V (DVP) It should be tied with nearby HGND by 1uF bypass capacitors.
A6	GENLOCK	BIO	-	External Frame sync input. Slave chip can receive the external frame sync signal from master chip/External Frame sync output. Master chip can output the external frame sync signal through this pad to synchronize all digital outputs of two or more chips. Multi-purpose pin function is supported. (ERR (Alarm)/UART Rx/PWM2/GPIO[8])
A7	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
A8	DGND/HGND /DGND_PLL	P	-	Digital (Core) GND I / O GND PLL GND
B1	NC	-	-	-
B2	AGND	P	-	Analog GND
B3	VSS	P	-	Digital(Core) GND
B4	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.

Ball	Ball Name	IO	Pull up/ Pull down	Ball Description
B5	X2	O	-	Master clock input pad (Crystal output)
B6	DVDD/ DVDD_PLL	P	-	Digital (Core) / PLL VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
B7	AGND	P	-	Analog GND
B8	AVDD	P	-	Analog VDD 3.0V It should be tied with nearby AGND by both 1uF bypass capacitors.
C1	ATEST	O	-	Analog test output
C2	AGND	P	-	Analog GND
C3	DGND	P	-	Digital(Core) GND
C4	DGND/HGND /DGND_PLL	P	-	Digital(Core) GND I / O GND PLL GND
C5	X1	I	-	Master clock input pad
C6	DVDD/ DVDD_PLL	P	-	Digital (Core) / PLL VDD 1.2V DC It should be tied with nearby DGND/DGND_PLL by 1uF bypass capacitors.
C7	REXT	O	-	External Resistor for MIPI
C8	HVDD	P	-	IO VDD 1.8V DC (MIPI), 1.8V (DVP) It should be tied with nearby HGND by 1uF bypass capacitors.
D1	AVDD	P	-	Analog VDD 3.0V It should be tied with nearby AGND by both 1uF bypass capacitors.
D2	DGND	P	-	Digital(Core) GND
D3	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
D4	VREFP3	O	-	VREFP3 output. It should be tied with nearby AGND by 1uF bypass capacitors.
D5	DGND/HGND /DGND_PLL	P	-	Digital(Core) GND I / O GND PLL GND
D6	DGND/HGND /DGND_PLL	P	-	Digital(Core) GND I / O GND PLL GND
D7	DN0/D1	O	-	MIPI DN0 Output / Digital Output bit 1
D8	DP0/D0	O	-	MIPI DP0 Output / Digital Output bit 0
E1	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
E2	VREFN1	O	-	VREFN1 output. It should be tied with nearby AGND by 1uF bypass capacitors.
E3	VREFP1	O	-	VREFP1 output. It should be tied with nearby AGND by 1uF bypass capacitors.
E4	PCLK	O	-	Digital Output Data can be latched by external devices at the rising or falling edge of PCLK
E5	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
E6	D6	O	-	Digital Output bit 6. Multi-purpose pin function is supported. (ERR (Alarm)/UART Rx/PWM2/GPIO[2])
E7	DN1/D3	O	-	MIPI DN1 Output / Digital Output bit 3
E8	DP1/D2	O	-	MIPI DP1 Output / Digital Output bit 2

Ball	Ball Name	IO	Pull up/ Pull down	Ball Description
F1	VREFP2	O	-	VREFP2 output. It should be tied with nearby AGND by 1uF bypass capacitors.
F2	VREFP4	O	-	VREFP4 output. It should be tied with nearby AGND by 1uF bypass capacitors.
F3	SPI_SS	O	-	Serial Peripheral Interface - Slave Select
F4	DGND/ HGND	P	-	Digital(Core) GND / IO GND
F5	DGND/ HGND	P	-	Digital(Core) GND / IO GND
F6	D9	O	-	Digital Output bit 9. Multi-purpose pin function is supported. (ERR (Alarm)/JTAG TMS/UART Tx/PWM1/GPIO[5])
F7	CKN/D5	O	-	MIPI Clock Negative Output / Digital Output bit 5
F8	CKP/D4	O	-	MIPI Clock Positive Output / Digital Output bit 4
G1	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
G2	SPI_MOSI	BIO	-	Serial Peripheral Interface - Master Output, Slave Input
G3	SPI_SCK	O	-	Serial Peripheral Interface - Serial Clock
G4	DVDD	P	-	Digital(Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
G5	HSYNC	O	-	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of int erest. It can be programmed to appear or not outside the vertical window of interest. M ulti-purpose pin function is supported. (ERR (Alarm)/JTAG TCK/UART Tx/PWM3/GPIO[7])
G6	MPP	BIO	-	Multi-purpose Pin Function Output (Digital Video Out(D11)/ERR (Alarm)/JTAG_TRSTn/UART Tx/PWM1/GPIO[1])
G7	D8	O	-	Digital Output bit 8. Multi-purpose pin function is supported. (ERR (Alarm)/JTAG TDO/UART Rx/PWM0/GPIO[4])
G8	D7	O	-	Digital Output bit 7. Multi-purpose pin function is supported. (ERR (Alarm)/UART Tx/PWM3/GPIO[3])
H1	SPI_MISO	BIO	-	Serial Peripheral Interface - Master Input, Slave Output
H2	SDA	BIO	-	2-wire serial interface clock, SDA line is pulled up to HVDD by off-chip resistor
H3	SCL	I	-	2-wire serial interface data, SCL line is pulled up to HVDD by off-chip resistor
H4	HVDD	P	-	IO VDD 1.8V DC (MIPI), 1.8V (DVP) It should be tied with nearby HGND by 1uF bypass capacitors.
H5	VSYNC	O	-	Vertical sync : Indicates the start of a new frame. Multi-purpose pin function is supported . (ERR (Alarm)/JTAG TDI/UART Rx/PWM2/GPIO[6])
H6	HVDD	P	-	IO VDD 1.8V DC (MIPI), 1.8V (DVP) It should be tied with nearby HGND by 1uF bypass capacitors.
H7	ERR	BIO	-	Safety error output. When a safety error occurs, '1' is output. Multi-purpose pin function is supported. (Digital Video Out(D10)/ERR (Alarm)/UART Tx/PWM0/GPIO[0])
H8	HVDD	P	-	IO VDD 1.8V DC (MIPI), 1.8V (DVP) It should be tied with nearby HGND by 1uF bypass capacitors.